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UTILITY PATENT APPLICATION TRANSMITTAL <small>(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))</small>	Attorney Docket No.	ATI-000152BT
	First Inventor or Application Identifier	Drapkin et al.
	Title	METHOD AND APPARATUS TO OPTIMIZE RECEIVING SIGNALS REFLECTION
	Express Mail Label No.	EL566349197US

APPLICATION ELEMENTS <small>See MPEP chapter 600 concerning utility patent application contents.</small>	ADDRESS TO: Commissioner for Patents Box Patent Application Washington, DC 20231
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3. <input checked="" type="checkbox"/> Drawing(s) (35 U.S.C. 113) [Total Sheets 5]	ACCOMPANYING APPLICATION PARTS 7. <input checked="" type="checkbox"/> Assignment Papers (cover sheet & document(s)) 8. <input type="checkbox"/> 37 C.F.R. § 3.73(b) Statement <input type="checkbox"/> Power of Attorney <small>(when there is an assignee)</small> 9. <input type="checkbox"/> English Translation Document (if applicable) 10. <input type="checkbox"/> Information Disclosure Statement (IDS)/PTO-1449 <input type="checkbox"/> Copies of IDS Citations 11. <input type="checkbox"/> Preliminary Amendment 12. <input checked="" type="checkbox"/> Return Receipt Postcard (MPEP 503) <small>(Should be specifically itemized)</small> 13. <input type="checkbox"/> * Small Entity Statement(s) <input type="checkbox"/> Statement filed in prior application, Status still proper and desired <small>(PTO/SB/09-12)</small> 14. <input type="checkbox"/> Certified Copy of Priority Document(s) <small>(if foreign priority is claimed)</small> 15. <input type="checkbox"/> Other: _____
4. Oath or Declaration [Total Pages 3] <ul style="list-style-type: none">a. <input checked="" type="checkbox"/> Newly executed (original or copy)b. <input type="checkbox"/> Copy from a prior application (37 C.F.R. § 1.63(d)) <small>(for continuation/divisional with Box 16 completed)</small><ul style="list-style-type: none">i. <input type="checkbox"/> <u>DELETION OF INVENTOR(S)</u> Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).	
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METHOD AND APPARATUS TO OPTIMIZE RECEIVING SIGNALS REFLECTION

BACKGROUND

The present invention relates to interconnected circuits operating at high frequency and, more particularly, to method and apparatus for compensating for impedance mismatch and reflection glitches which occur due to charging or discharging of an input receiver parasitic capacitor by the positive/negative going edges of the high frequency input signal.

The charging/discharging of the input receiver parasitic capacitor causes an additional impedance mismatch, and a reflection glitch. Stated in another way, in the presence of a rising edge signal of high frequency, this change will charge the parasitic capacitor. The energy used to charge the capacitor is derived from the signal inputted in the input/output device, causing the signal to be distorted. Distortion also occurs during the negative going edge of a high frequency signal similarly causing signal distortion due to discharge of the parasitic capacitor that likewise disturbs the signal.

To date, there is no technique for providing compensation for matching the line impedance because of charge/discharge of an input receiver parasitic capacitor.

SUMMARY

The present invention is characterized by comprising a method and apparatus for detecting variations in charge/discharge of an input parasitic capacitor and compensating for the detected condition by respectively discharging/charging said capacitor to eliminate or significantly reduce reflection glitches.

The charging/discharging detection circuit selectively controls circuitry for preventing the parasitic capacitor from drawing energy from the input signal during the occurrence of a rising edge and conversely prevents withdrawal and discharge from the

parasitic capacitor in the presence of a negative-going input (falling edge), in order to assure impedance matching and to prevent a reflection glitch.

The detection and control circuitry may comprise an integrated circuit or any other electronic circuit to accomplish the desired result.

5 It is therefore, one object of the present invention, is to provide an apparatus for compensating for impedance mismatch between interconnected circuits operating at high frequencies.

Another object of the present invention is to provide method and apparatus for preventing reflection glitches that occur due to the presence of parasitic capacitance at the
10 input of a circuit receiving a high frequency signal.

Still another objection of the present invention is to provide method and apparatus for compensating for impedance mismatch between interconnected circuits by detecting the occurrence of charging/discharging of a parasitic capacitance at an input of the receiving circuit and utilizing the detected condition to respectively prevent energy from
15 being withdrawn from/introduced into the input signal to the receiving circuit, thereby prevent reflection glitches.

BRIEF DESCRIPTION OF THE DRAWINGS

The above, as well as other objects of the present invention will become apparent when reading the accompanying description and drawings in which:

20 Figures 1A and 1B show simplified circuit diagrams useful in explaining the impedance mismatch problems occurring in interconnected circuits operating at high frequency.

Figures 2A, 2B, 2C and 2D show simplified circuit diagrams of embodiments of the present invention that are useful in explaining the operation and capabilities of the
25 present invention.

Figure 3 shows an additional embodiment of the present invention.

Figure 4 shows a timing diagram to understand Figure 3 schematic.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Transmitter output impedance and transmission line impedance matching and termination technique is a concern if the signals rising/falling timing is comparable with the flight time through transmission line. In some electronic interfaces, it is very important that the impedance of a transmitter match the characteristic line impedance and that a receiver connected thereto be capable of operating like an open circuit. Still other interfaces employ additional line termination techniques in order to prevent from reflection at the receiving end. In the latter case, the additional terminated device or devices can be installed at the receiving end to minimize possible sources of reflection.

In some interfaces, it is recommended that both the transmitter and receiver be provided with terminations.

One of the main problems encountered in such devices is a receiver parasitic capacitor.

An input/output pad of a circuit receiver, when in the receiving mode, typically has disabled output buffers as well as some additional electronic devices that provide significant receiver input capacitance. In such case, additional current will be taken from (be sent to) the input signal to charge/discharge the parasitic capacitor, which causes impedance mismatch and reflected glitches resulting in distortion of the input signal. Although it is well-known to use serial or parallel termination devices (such as resistors, transistors, etc.) between the transmitter and the receiver to minimize the transmission line characteristic impedance mismatch, prior to the present invention there was no technique or apparatus known to these inventors that can provide additional receiver parasitic capacitor compensation to match the line impedance.

Reference will now be made to Figures 1A and 1B which aid in an understanding of the problems resolved by the method and apparatus of the present invention.

Figure 1A shows a simplified serial circuit termination arrangement in which a transmitter T (represented by a switch to power or ground, and transmitter output impedance) is coupled through a transmission line to an input/output (I/O) pad P of a

receiver R, the example being when the input/output device is operating as a receiver. C_p represents an input pad parasitic capacitor.

In the serial termination case shown in Figure 1A, when the output impedance of the transmitter Z_{TR} matches the transmission line impedance Z_L the receiver R may be treated as an open circuit and there is optimum transfer of the transmitted signal to the receiver.

Figure 1B shows the parallel termination case wherein the terminated resistor R_{TERM} is selected to have an impedance value which is equivalent to the impedance of the transmission line Z_L in order to prevent signal reflection back to the transmitter. These terminations are conventional.

At high operating frequencies, it cannot be assumed that the input of the receiver R is an open circuit into the presence of an input parasitic capacitor in order to be able to treat the receiver R as an open circuit, the signal applied to the input of the receiver R is to charge/discharge the parasitic capacitor. Such charging/discharging means that the signal that is received by the receiver R will be distorted. The same situation occurs with the parallel termination shown in Figure 1B wherein a terminating resistor R_{TERM} is in parallel with the parasitic capacitance C_p . In addition, the higher the frequency, the greater the distortion. This distortion is particularly referred to as a "glitch" when the receiver has to have a strong signal and a spike is heard as a result of the distortion.

In the case where the incoming signal has a rising edge, the parasitic capacitor is charged at this time. The energy is taken from the input signal to charge the capacitor causes distortion of the input signal.

However, by providing a tracking or detecting circuit capable of providing additional current to charge the capacitor without taking energy out of the input signal to provide for such charge, it is possible to prevent or significantly reduce distortion of the input signal.

In the case where the signal is a negative going edge, capacitor C_p at such time is already charged and will be discharged causing a disturbance of the signal. By use of the

tracking device, the parasitic capacitor is prevented from discharging into the receiver thereby preventing a disturbance of the input signal and preventing "glitches".

Summarizing, in the presence of a parasitic capacitance at the input circuit of the receiver, the charge/discharge of the parasitic capacitance occurring during the presence
5 of a negative or positive going edge causes distortion of the input signal.

Charging/discharging of the parasitic capacitance C_p results in a current which is given by $i = Cdv/dt$. By tracking the current through the parasitic capacitance, it is possible to determine the rate of change of charge, i.e. positive or negative (charging or discharging). Determining the magnitude and direction of the current may be
10 accomplished by a tracking system shown in Figure 2A which magnitude and direction is utilized to provide compensation for the charging/discharging of the parasitic capacitor C_p so that, for example, when the signal has a positive going edge, tracking system 10 provides the charging for the parasitic capacitor that would otherwise be derived from the input signal to prevent distortion of the input signal. Conversely, when the tracking
15 system 10 detects a negative going edge, the tracking system prevents the parasitic capacitor from discharging into the input signal thereby preventing distortion during either positive going or negative going edges of the input signal.

Figure 2B shows slightly more detailed schematic as compared with Figure 2A, in which the tracking system 10 is a dv/dt analyzer operating a charge pump 11 to
20 compensate for charging or discharging of parasitic capacitor C_p .

With reference to Figure 2C, the input signal is shown applied to the I/O pad P through the transmission line represented by the impedance Z_L . The tracking system employs a capacitor C_T having one terminal coupled to one terminal of the parasitic capacitance C_p and the other terminal coupled between a current source 12 and an NMOS
25 transistor 14 having its gate coupled its drain, as well as with the gate of the second NMOS transistor 16. A PMOS transistor 18 has its drain and gate coupled to a drain of NMOS transistor 16 as well as with the gate of the second PMOS transistor 20.

In operation, during a rising edge signal ($+dv/dt$), since the voltage of C_T cannot change instantaneously, the voltage increases at terminal 22 which ultimately causes the

drain of PMOS transistor 20 to provide sufficient current at terminal 24 to compensate for a portion of the current that would otherwise be provided to parasitic capacitance C_T by the input signal.

During the negative edge of the signal ($-dv/dt$), the voltage instantaneously decreases at terminal 22 which ultimately causes the transistor 20 to prevent the voltage level of terminal 24 to be reduced, thereby preventing occurrence of a glitch during the negative going portion of the input signal.

Figure 2D shows still another embodiment of the present invention, NMOS output buffer transistor 26 being used as a parallel termination device. In this embodiment, under DC conditions, i.e. when an input signal is constant (high or low), the input impedance Z_i is defined by the impedance of the circuit that includes NMOS transistor 26 having an impedance Z_B in parallel with either the impedance Z_C of the circuit that includes NMOS transistor 28 or the circuit including NMOS transistor 30 with the impedance Z_D . More specifically, when an input DC level is low, the value of input impedance is given by equation (1) ($Z_i = Z_B || Z_D$). When an input DC level is high, the value of input impedance is given by equation (2) ($Z_i = Z_B || Z_C$).

When the signal is changing and goes from a low level to a high level, the impedance is given by equation (3) ($Z_i = Z_B || Z_E$), where Z_E is an input pad parasitic capacitor impedance. When the level changes from high to low, the impedance is given by equation (4) ($Z_i = Z_B || Z_E || Z_C || Z_D$).

In the AC case, the rising signal edge inverter 32 will turn "OFF" NMOS transistor 30, but inverter 34 within some time could not turn "ON" NMOS transistor 28 because of Delay Line 36. Delay Line 36 is chosen to delay NMOS transistor 28 to be "ON" until an input pad parasitic capacitor C_p will be charged and could not interfere with termination. As soon as $|Z_E| = |Z_C| = |Z_D|$ an input pad impedance should not be different during DC low level condition, low to high AC condition, and DC high level condition.

In the AC case, the falling signal edge inverter 32 will turn "ON" NMOS transistor 30, but inverter 34 within some time could not turn "OFF" NMOS transistor 28

because of Delay Line 36. Delay Line 36 is chosen to delay NMOS transistor 28 to be "OFF" until an input pad parasitic capacitor C_p will be discharged through this NMOS transistor 28 and could not interfere with termination.

Another embodiment of the invention is shown in Figure 3 that employs digital logic circuits 40 through 54, PMOS transistor 56 and NMOS transistor 58.

During occurrence of a positive edge of the input signal, transistor 56 provides current to terminal 60 (voltage pulse at the node H, Figure 4, that is the gate of transistor 56), and transistor 58 is not conducting, due to the logic circuitry (low voltage at node G, Figure 4, that is the gate of transistor 58).

During the occurrence of a negative edge of the input signal, transistors 58 and 56 are respectively conducting (voltage pulse at node G, Figure 4, that is the gate of transistor 58) and non-conducting (high voltage at node H Figure 4, that is the gate of transistor 56) to prevent the parasitic capacitance from discharging current into the input signal source.

The embodiment of Figure 3 employs two different thresholds (switching points) for the inverters 40 and 42. Figure 3 shows an input signal with positive and negative edges and an intervening constant level. The inverter 42 switching point is lower compared with the inverter 40 switching point. That means at the rising signal edge the inverter 42 will be switched first, and the inverter 40 will be switched later. During the falling signal edge the inverter 40 will be switched first, and the inverter 42 will be switched later (Figure 4, nodes A and B). The Figure 3 schematic employs logic circuits (44, 46, 48, 50, 52, and 54) to detect a direction of change in voltage of input signal (low to high, or high to low), and based upon the detected direction, provides short pulses at the gates of NMOS transistor 58 (node G) and PMOS transistor 56 (node H) during the rising and falling edges of an input signal to compensate the parasitic input capacitor charge/discharge current.

* * *

CLAIMS

What is claimed is:

1. A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of:

detecting a direction of change in voltage of said input signal; and

5 introducing a current to said parasitic capacitance to compensate for current of said input signal charging said parasitic capacitance responsive to detection of a positive edge of said input signal.

2. The method of claim 1, wherein said signal is applied to an input of an input/output device.

3. A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of:

detecting a direction of change in voltage of said input signal; and

5 preventing discharge of said parasitic capacitance responsive to detection of a negative edge of said input signal.

4. A method for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance, comprising the steps of:

detecting a change in voltage of said input signal; and

5 changing an impedance of a parallel termination circuit that is in parallel with said parasitic capacitance to reduce distortion of said input signal.

5. Apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance, comprising:

a detection circuit for detecting a change in voltage of said input signal coupled to said input; and

5 a correction circuit coupled to said detection circuit for compensating for current from said input signal that would be diverted to said parasitic capacitance due to a positive edge of said input signal.

6. The apparatus of claim 5, wherein said detection circuit includes a capacitance.

7. The apparatus of claim 5, wherein said circuit is an input/output device.

8. Apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance, comprising:

 a detection circuit for detecting a change in voltage of said input signal coupled to said input; and

5 a correction circuit coupled to said detection circuit for compensating for preventing current from said parasitic capacitance to be added to said input signal due to a negative edge of said input signal.

9. The apparatus of claim 8, wherein said detection circuit includes a capacitance.

10. The apparatus of claim 8, wherein said circuit is an input/output device.

11. Apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance, comprising the steps of:

 a detecting circuit for detecting a change in voltage of said input signal; and

5 a correction circuit for changing an impedance of a parallel termination circuit that is in parallel with said parasitic capacitance to reduce distortion of said input signal.

12. A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of:

detecting a direction in change in voltage of said input signal; and

5 introducing a current to said parasitic capacitance to compensate for distortion of said input signal due to said parasitic capacitance responsive to detection of a positive edge of said input signal.

13. A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of:

detecting a direction of change in voltage of said input signal; and

5 preventing introduction of a current from said parasitic capacitance into said input signal responsive to detection of a negative edge of said input signal.

14. Apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance, comprising:

a first circuit element for selectively providing current to said parasitic capacitance;

5 a second circuit element for selectively preventing discharge of said parasitic capacitance into said input; and

a control circuit monitoring said input signal for respectively turning on said first circuit element and turning off said second circuit element when a positive going edge of said input signal is detected and for turning off said first circuit element and turning on
10 said second circuit element when a negative going edge of said input signal is detected.

15. The apparatus of claim 14 wherein said first and second circuit elements have a common terminal coupled to said parasitic capacitance.

16. The apparatus of claim 15 wherein said first and second circuit elements are transistors.

17. The apparatus of claim 16 wherein one of said transistors is a PMOS transistor and another one of said transistors is an NMOS transistor.

ABSTRACT

An input/output circuit in a receiving mode typically has disabled output buffers as well as other electrical components that provide significant receiver input capacities at high operating frequencies. A detection circuit detects the charging/discharging of the parasitic capacitance and operates a regulating circuit to compensate for the charging/discharging of the parasitic capacitance during rising/falling edges of an input signal, thereby correcting for impedance mismatch and reflection glitches.

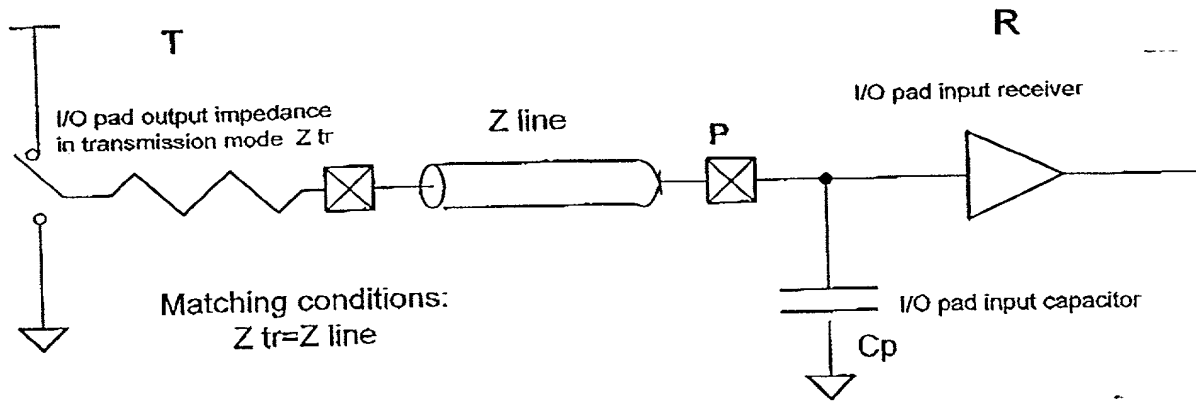


Fig1A. Serial termination

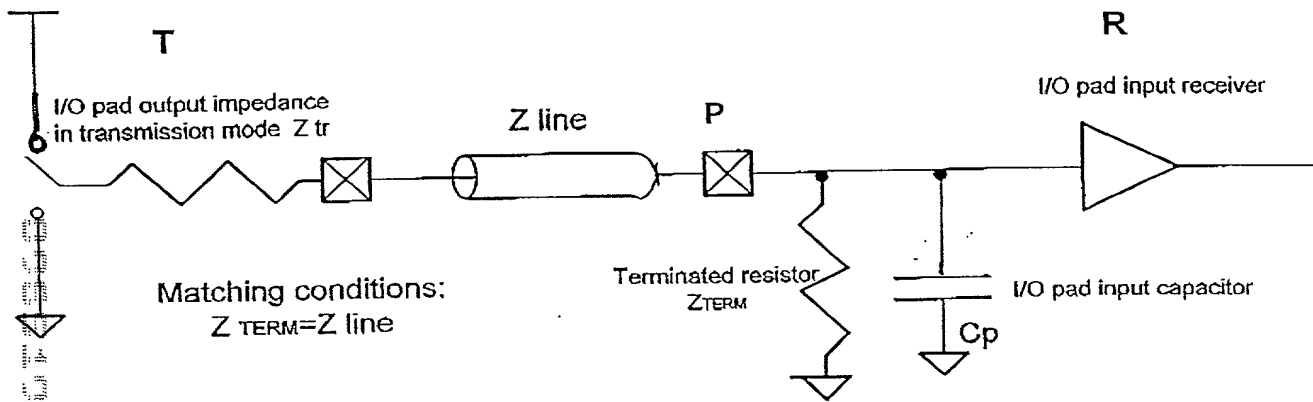


Fig1B. Parallel termination

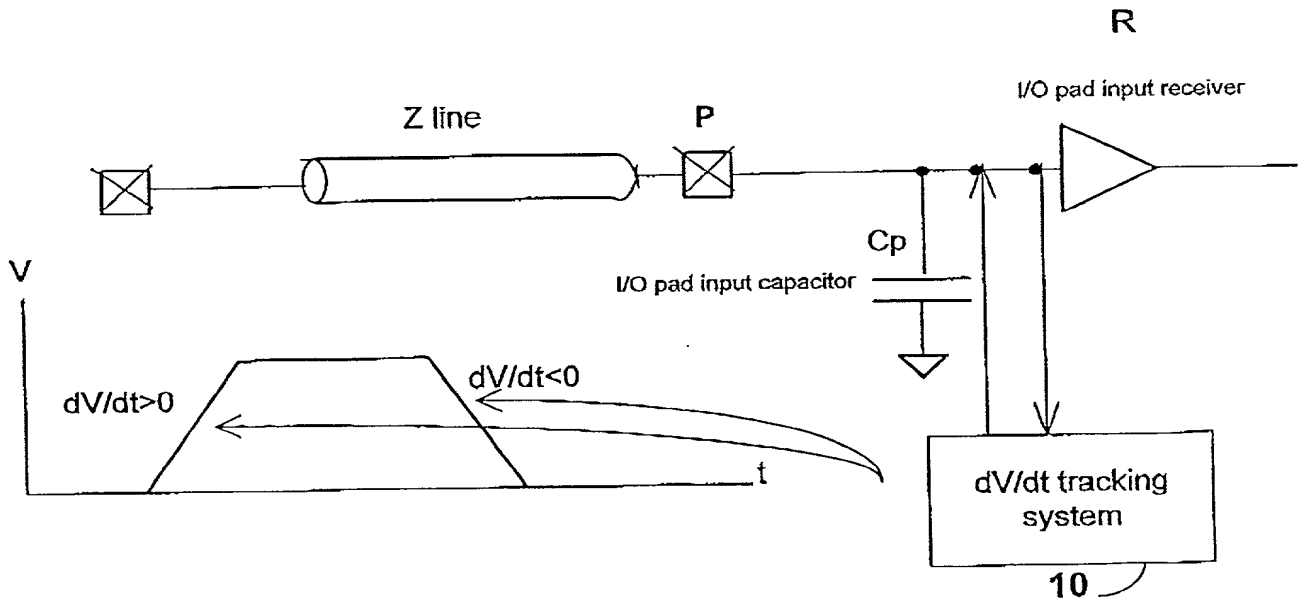


Fig2A. dV/dt tracking system

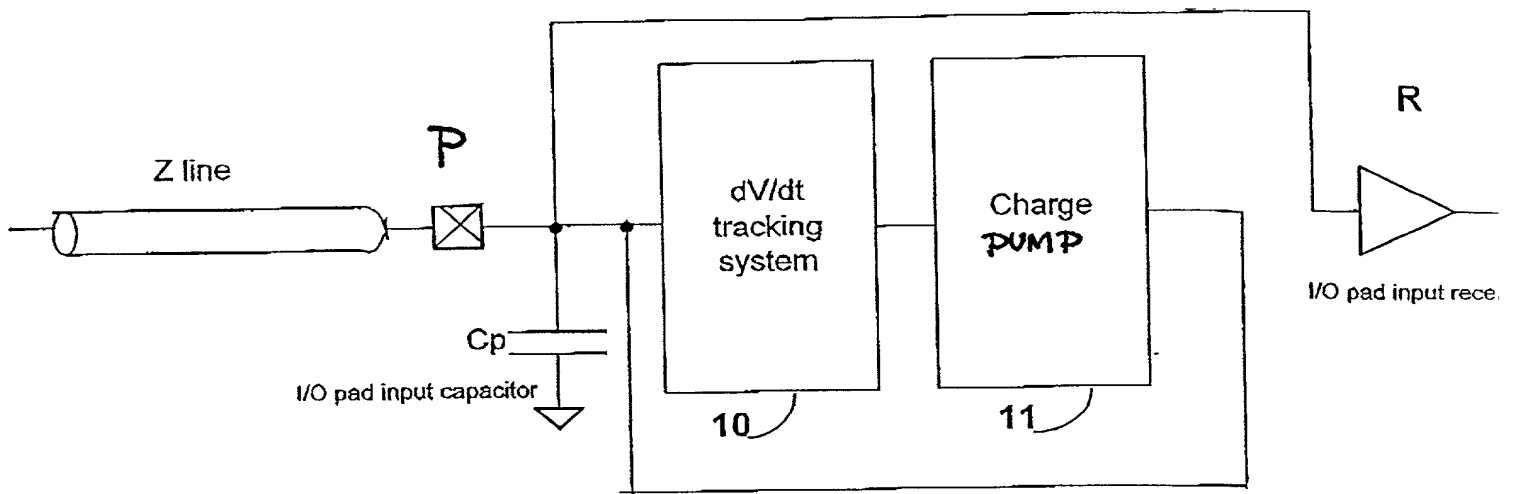


Fig. 2B dV/dt tracking system with charge pump

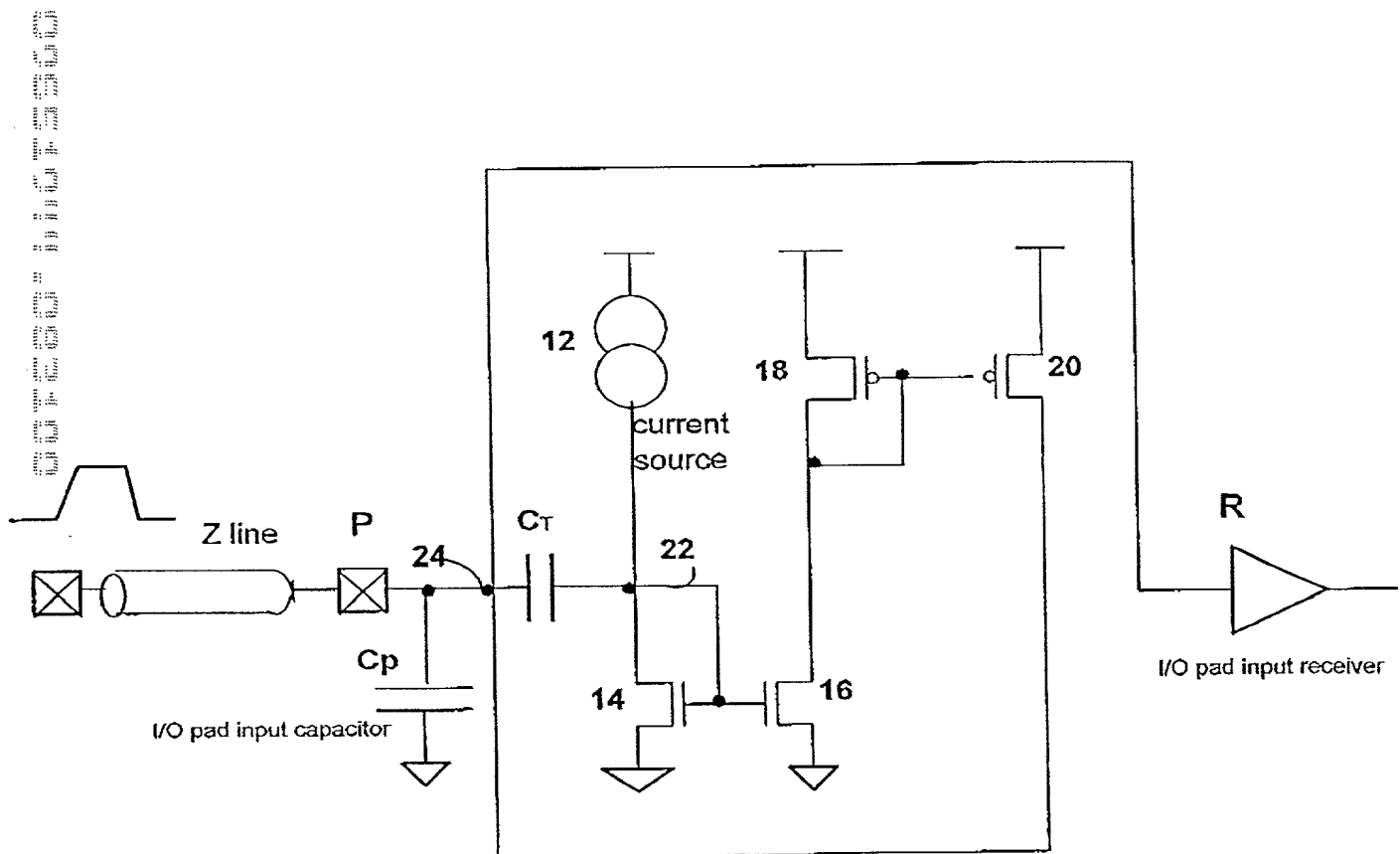
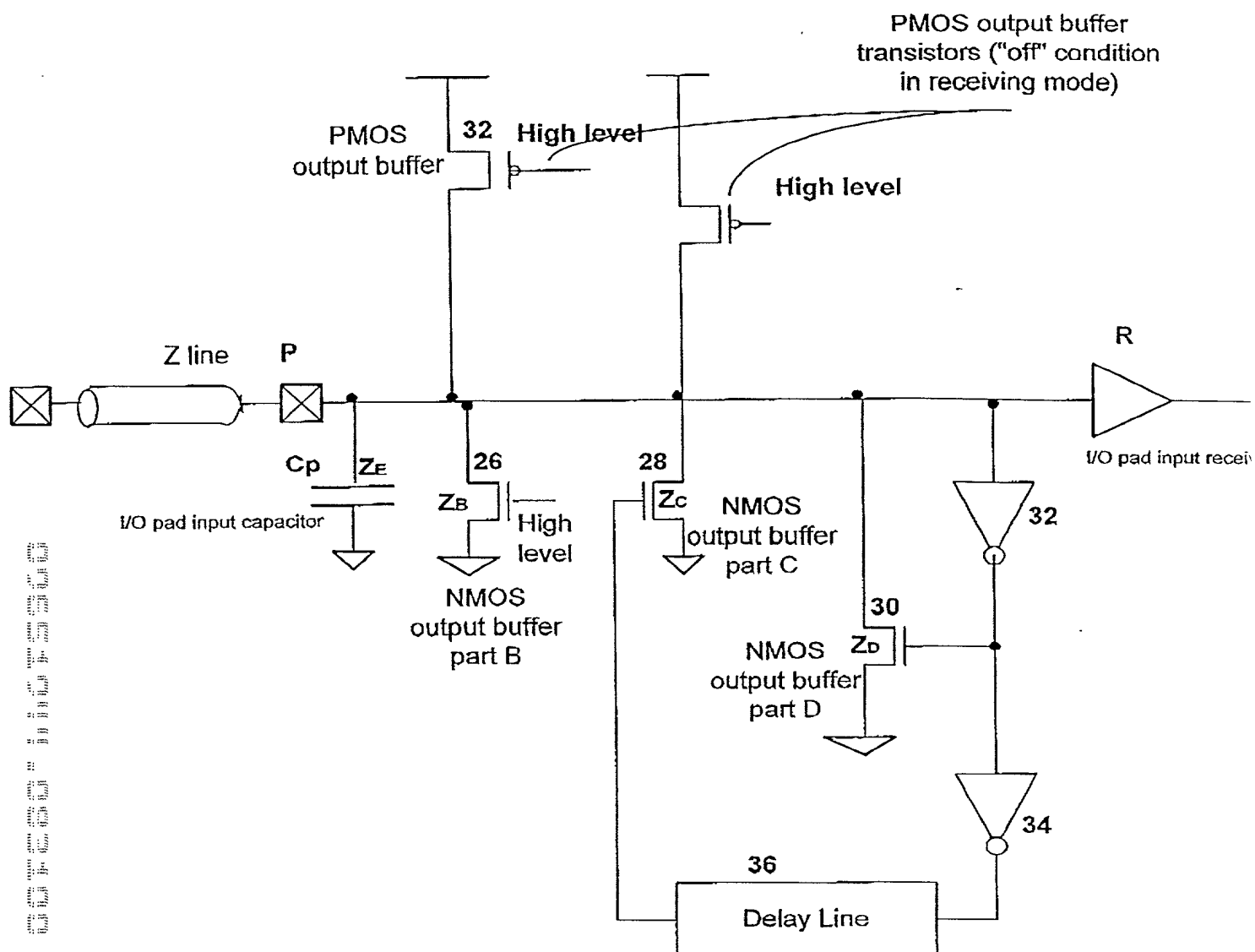


Fig. 2C. dV/dt tracking system with charge pump (more detailed)



$$Z_{\text{input}} = Z_B \parallel [Z_C(\text{or } Z_D, \text{or } Z_E)]$$

if $|Z_C| = |Z_D| = |Z_E|$, then an input signal can not change Z_{input}

Fig. 2D NMOS output buffer parallel termination

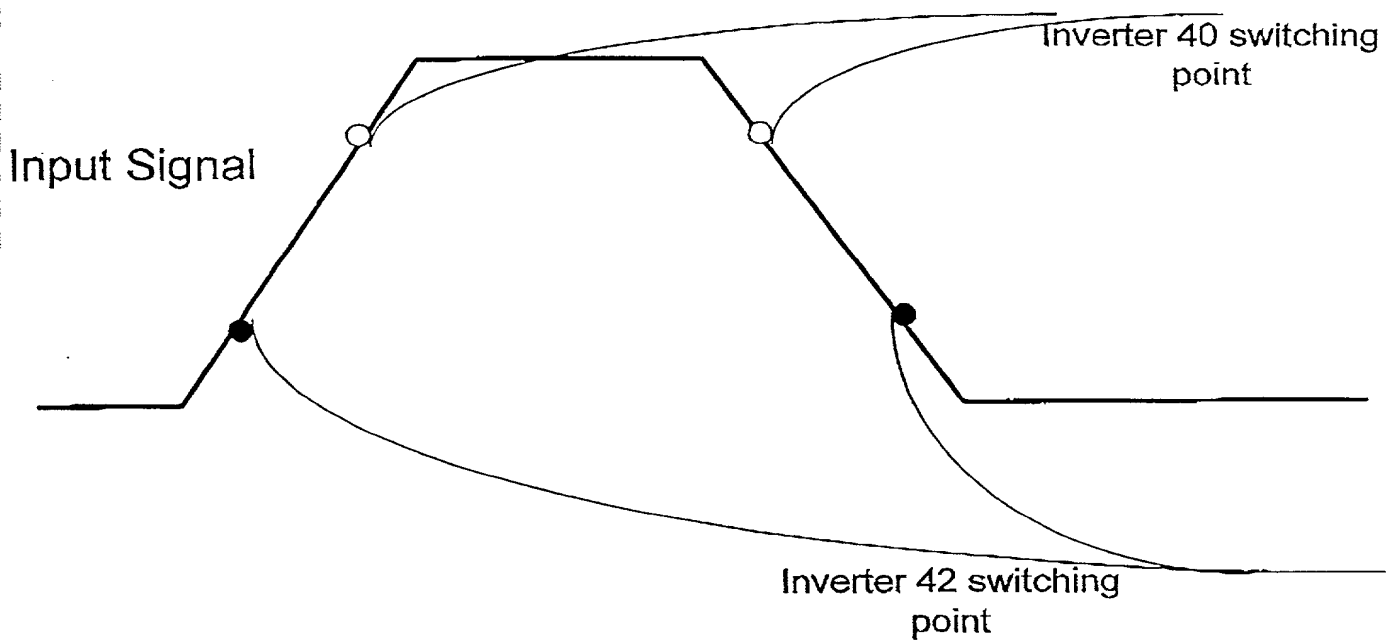
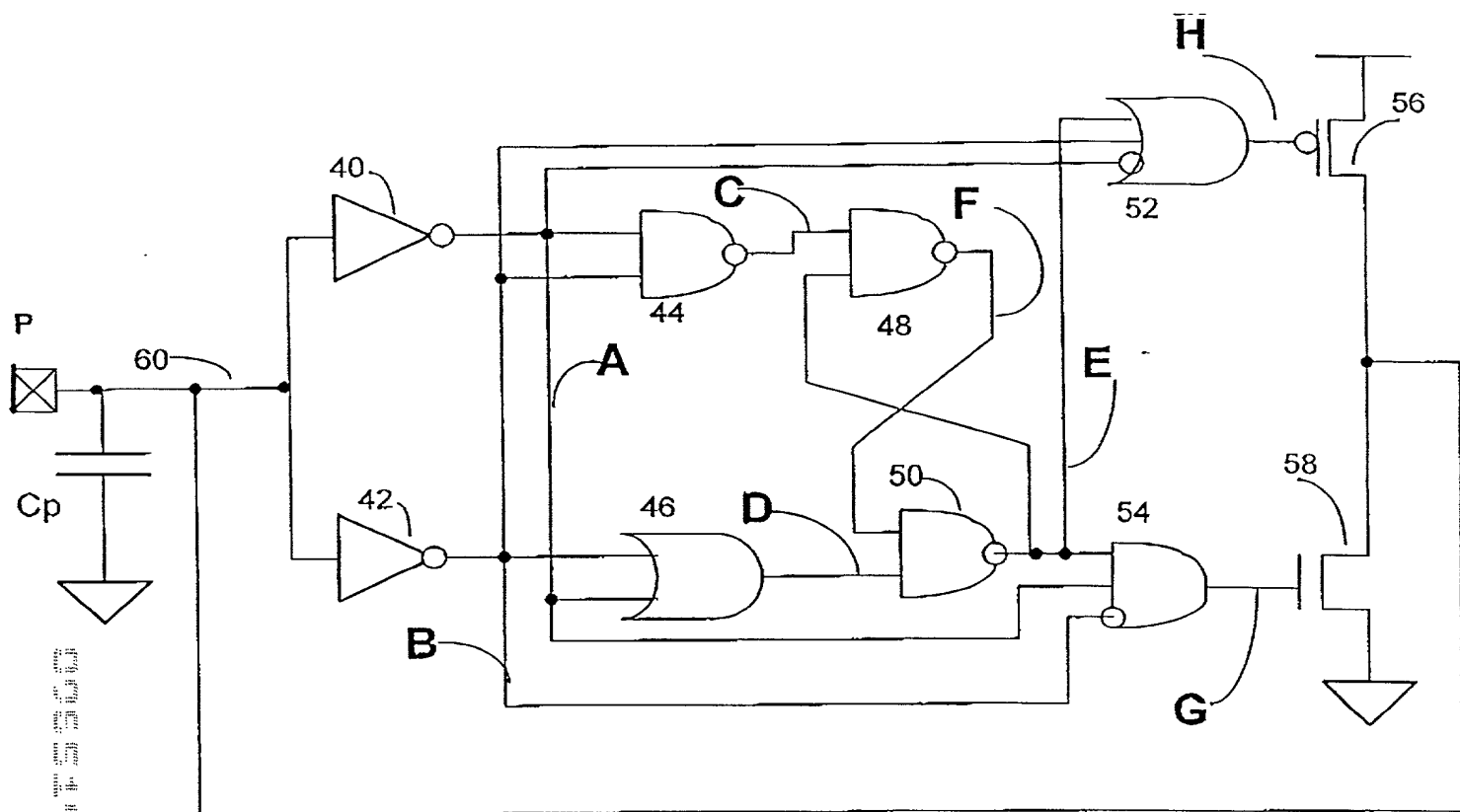


Fig. 3. An input parasitic capacitor charge/discharge circuit

Input Signal

Node A

Node B

Node C

Node D

Node E

Node F

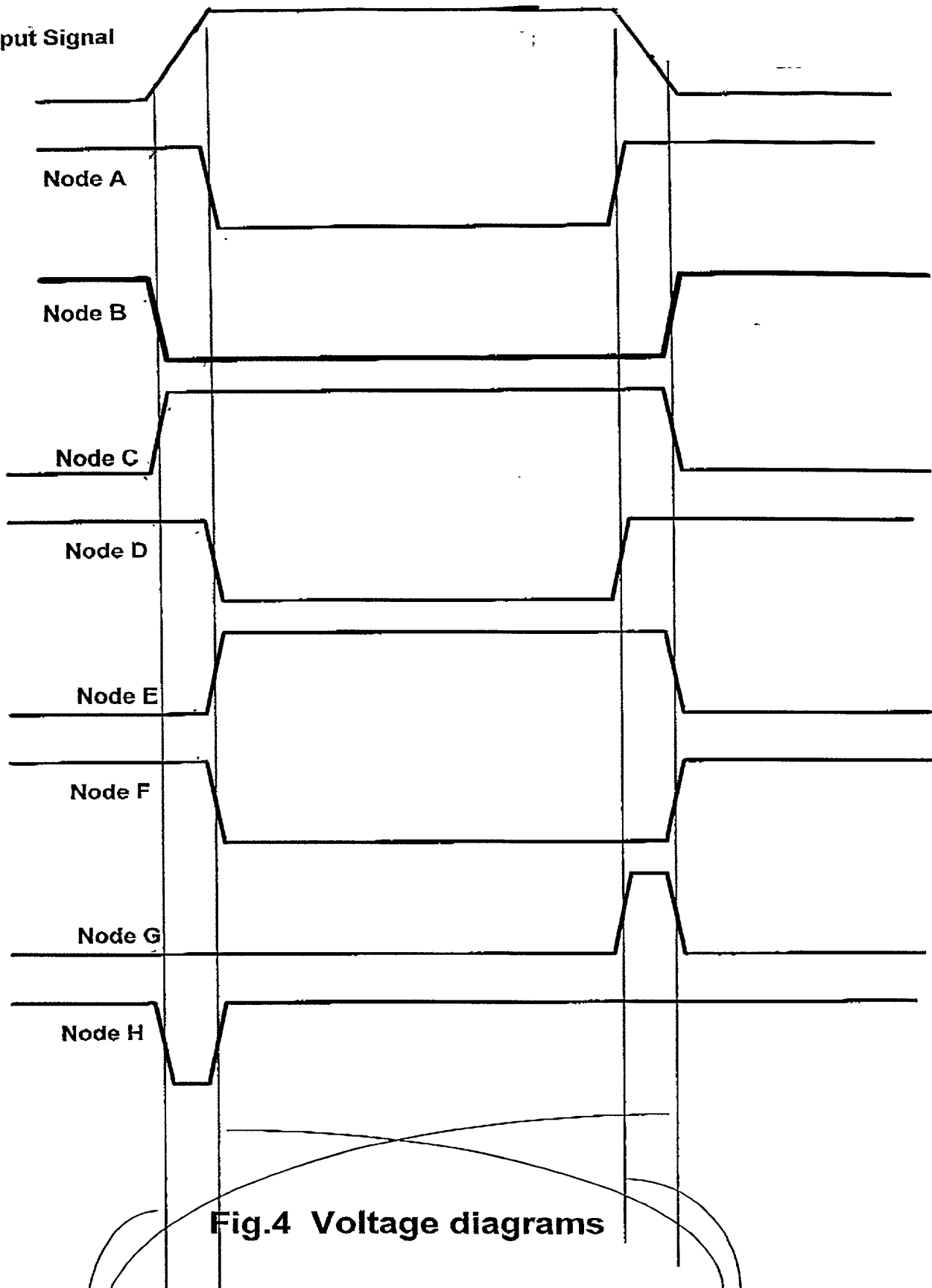
Node G

Node H

Fig.4 Voltage diagrams

Inverter 42 switching point

Inverter 40 switching point



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	First Named Inventor	Drapkin et al.	
	<i>COMPLETE IF KNOWN</i>		
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	Filing Date	Not Yet Known	
	Group Art Unit	Not Yet Known	
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U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)

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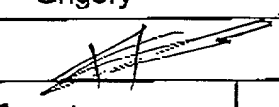
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☒ Additional Inventors are being named on the 1 supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto

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DECLARATION**ADDITIONAL INVENTOR(S)**
Supplemental Sheet
Page 1 of 1

Name of Additional Joint Inventor, if any:				<input checked="" type="checkbox"/> A petition has been filed for this unsigned inventor			
Given Name (first and middle [if any])				Family Name or Surname			
Grigory				Temkine			
Inventor's Signature						Date	31.08.00
Residence: City	Toronto	State	Ontario	Country		Citizenship	Russia
Post Office Address 125 Neptune Drive, #404							
Post Office Address							
City	Toronto	State	Ontario	ZIP	M6A 1X3	Country	Canada
Name of Additional Joint Inventor, if any:				<input type="checkbox"/> A petition has been filed for this unsigned inventor			
Given Name (first and middle [if any])				Family Name or Surname			
Inventor's Signature						Date	
Residence: City		State		Country		Citizenship	
Post Office Address							
Post Office Address							
City		State		ZIP		Country	
Name of Additional Joint Inventor, if any:				<input type="checkbox"/> A petition has been filed for this unsigned inventor			
Given Name (first and middle [if any])				Family Name or Surname			
Inventor's Signature						Date	
Residence: City		State		Country		Citizenship	
Post Office Address							
Post Office Address							
City		State		ZIP		Country	

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